EAST - [kevin's workspace.wsp:1]

File View Edit Tools Window Help

- Drafts
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- Active
  - L1: (37) (writ$4 or stor$4) with response with (read adj miss)
  - L2: (0) polymer adj (ferroelectric or (ferro adj electric)) adj cache
  - L3: (7) polymer adj (ferroelectric or (ferro adj electric)) adj memory
  - L4: (1) polymer near5 (ferroelectric or (ferro adj electric)) near5 cache
  - L5: (95) polymer near5 (ferroelectric or (ferro adj electric)) near5 memory
  - L6: (157) polymer adj (ferroelectric or (ferro adj electric))
  - L7: (143476) nonvolatile or (non adj volatile)
  - L8: (16) 6 with 7
- Failed
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	U		Document ID	Issue Date	Inventor	Current OR	Pages	
1	☐	☑	US 20020160116 A1	20021031	Nordal, Per-Erik et al.	427/378	6	M f

BRS form | IS&R form | Hits | Details | HTML

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NUM

DOCUMENT-IDENTIFIER: US 20030061436 A1

TITLE: Transportation of main memory and intermediate memory contents

--------- KWIC --------

Detail Description Paragraph - DETX (5):
[0015] The nonvolatile memory array 18 that is part of memory module 12 may be any type of persistent memory, one that retains its contents even after loss of power. A particularly well-suited memory technology for the context of this invention is polymer ferroelectric memory arrays. Generally, this type of memory comprises a layer of polymer material having ferroelectric properties sandwiched between layers of metal. The layers of metal are patterned to define word lines and bit lines as are commonly used in addressing memory cells. The region of polymer between the word line and bit line cross over points become the memory cells. Manipulation of the voltages on the word lines and bit lines can causes changes in the polarization state of the ferroelectric polymer, with one state being defined as a data `1` and the opposite polarization state being defined as a data `0.`

Detail Description Paragraph - DETX (6):
[0016] The polymer ferroelectric memories generally do not require separate circuits of transistors for each cell. Therefore, they are simpler to manufacture, as well as denser in population. This provides a large capacity, nonvolatile memory array that is not very expensive. Other types of nonvolatile memory are also within the scope of the invention, including volatile memory with a battery backup, as the battery will prevent the memory from losing its contents when the main power is turned off. Such a large, nonvolatile memory array provides opportunities in management of memory in various types of system that were not previously available.

Claims Text - CLTX (3):
2. The nonvolatile memory module of claim 1, wherein the nonvolatile memory array further comprises a polymer ferroelectric memory array.

US 20030061436A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2003/0061436 A1**

Royer, JR. et al. (43) **Pub. Date: Mar. 27, 2003**

(54) **TRANSPORTATION OF MAIN MEMORY AND INTERMEDIATE MEMORY CONTENTS**

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(21) Appl. No.: **09/963,185**

(22) Filed: **Sep. 25, 2001**

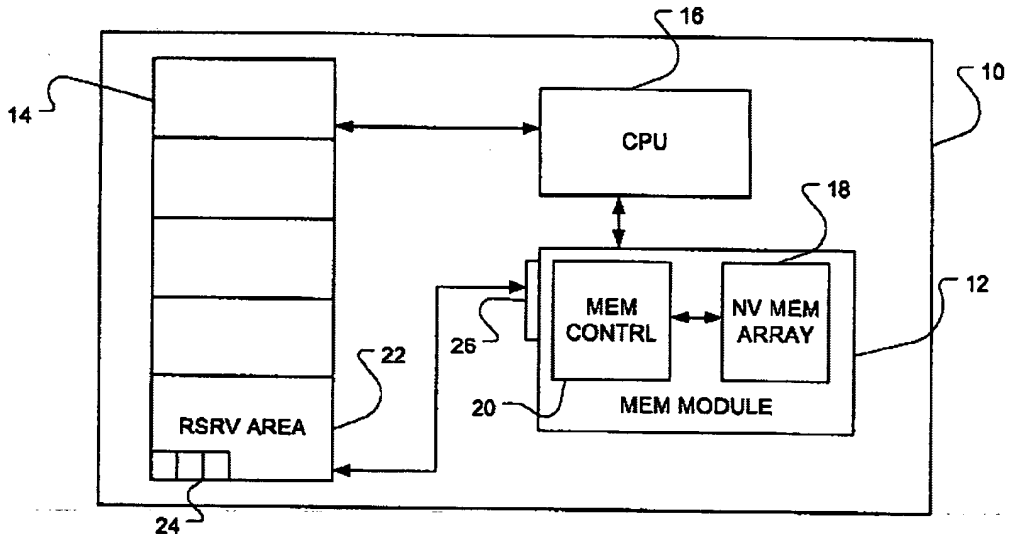
Publication Classification

(51) **Int. Cl.**[7] **G06F 13/00**

(52) **U.S. Cl.** **711/103**

(57) **ABSTRACT**

A nonvolatile memory module. The module includes a nonvolatile memory array and a connector allowing the array to make connection with a host system. A memory controller operates to either create an image of a nonvolatile intermediate memory in response to an imaging request or populate a nonvolatile intermediate memory in response to an installation request.



DOCUMENT-IDENTIFIER: US 20020160116 A1

TITLE: Method for the processing of ultra-thin polymeric films

--------- KWIC --------

Summary of Invention Paragraph - BSTX (3):

[0003] Hitherto, the ferroelectric polymers have been used commercially in sensors and activators that exploit the piezo- and pyroelectric effects in these materials, but these polymers and other classes of polymers with ferroelectric or electret properties are now also being developed for use as memory films in non-volatile data storage devices. In the latter case, data are stored by polarizing a thin film of the polymer in the direction normal to a supporting surface, a logic "1" being represented by, e.g. a polarization vector in the material pointing down towards the supporting surface, and a logic "0" by a polarization vector in the opposite direction. As shall be explained below, data storage applications require polymer films that are extremely thin, typically one to two orders of magnitude thinner than those used in present-day sensors and actuators. Thus, technologies and processes developed by the industry for manufacturing the sensors and actuators are inadequate for the new data storage devices.

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(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2002/0160116 A1**

Nordal et al. (43) **Pub. Date: Oct. 31, 2002**

(54) **METHOD FOR THE PROCESSING OF ULTRA-THIN POLYMERIC FILMS**

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(21) Appl. No.: **09/958,339**

(22) PCT Filed: **Feb. 6, 2001**

(86) PCT No.: **PCT/NO01/00040**

(30) **Foreign Application Priority Data**

Feb. 29, 2000 (NO) 20001025

Publication Classification

(51) **Int. Cl.**[7] **B05D 3/02**; B05D 3/04

(52) **U.S. Cl.** **427/378**; 427/384

(57) **ABSTRACT**

In a method for preparing ultra-thin films of carbon-containing materials, particularly thin films of polymer materials. Films with a thickness of 0.5 μm or less are formed by deposition of the materials from a liquid phase onto a solid surface. The deposition takes place in an enclosure where the materials also are subjected to a post-deposition processing. The total humidity content in the enclosure shall be maintained at a level corresponding to a relative humidity of less than 50% in a volume of air equal to the volume of enclosure by excluding and/or removing water arid water vapor from the materials and/or the atmosphere in the enclosure.

DOCUMENT-IDENTIFIER: US 20010038104 A1

TITLE: MULTILAYER MATRIX-ADDRESSABLE LOGIC DEVICE WITH A PLURALITY OF INDIVIDUALLY MATRIX-ADDRESSABLE AND STACKED THIN FILMS OF AN ACTIVE MATERIAL

-------- KWIC --------

Summary of Invention Paragraph - BSTX (6):

[0006] Applied as a memory medium, i.e. for storage of data, the functional medium 1, as shown in FIGS. 1 and 2 according to prior art, responds to electrical stimuli which effect a reversible or an irreversible change in the physical or chemical properties, which represents a given logical state, for instance a binary 1 or 0, and which can be detected by suitable means as the complex impedance between the electrodes or as the transmitting or reflecting optical properties of the memory medium or functional medium. Examples of reversible memory mediums which can be used in erasable and rewriteable memories are liquid crystals, metal-organic compounds, doped polymers and ferroelectric materials. Examples of irreversible memory materials which can be used in read only memories (ROM), or memories of the WORM type (Write Once Read Many Times) are polymers which are doped in order to obtaine a controllable electrical rectification and conductance.

US 20010038104A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2001/0038104 A1**

GUDESEN et al. (43) **Pub. Date: Nov. 8, 2001**

(54) **MULTILAYER MATRIX-ADDRESSABLE LOGIC DEVICE WITH A PLURALITY OF INDIVIDUALLY MATRIX-ADDRESSABLE AND STACKED THIN FILMS OF AN ACTIVE MATERIAL**

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(*) Notice: This is a publication of a continued prosecution application (CPA) filed under 37 CFR 1.53(d).

(21) Appl. No.: **09/255,579**

(22) Filed: **Feb. 22, 1999**

(30) **Foreign Application Priority Data**

Feb. 25, 1998 (NO) 980781

Publication Classification

(51) **Int. Cl.**[7] **H01L 23/495**; H01L 29/74; H01L 31/111

(52) **U.S. Cl.** **257/149**; 257/676

(57) **ABSTRACT**

In a multilayer logic device or processor device with a plurality of individually matrix-addressable stacked thin layers of an active material, the active material in each layer is provided between a first electrode set and a second electrode set wherein the electrodes in the first set realize the columns and the electrodes in the second set the rows in an orthogonal array. The intersections between the electrodes in the array define logic cells in the layer of active material, and the stacked layers of active material are provided on a common supporting substrate. A separation layer with determined electrical or thermal properties is provided between each layer of active material.